

Ranit Gorai

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Portfolio LeetCode

Professional Summary

Analytically driven Electronics & Telecommunication Engineering student with hands-on experience in Python, SQL, and data structures & algorithms, complemented by research exposure to advanced computational methods and protocol design at a premier research institute (IISc Bangalore). Skilled at breaking down complex, unstructured problems into structured, implementable frameworks. Strong foundation in DBMS/SQL, analytical reasoning, and a growth mindset oriented toward continuous learning of new tools, algorithms, and business domains. Seeking to apply strong problem-solving, coding, and analytical rigor to deliver data-driven insights as an Associate Data Analyst.

Education

2023–Present **B.E. in Electronics and Telecommunication Engineering**, Jadavpur University, Kolkata, India
2023 **AISSCE (PCM)**, DAV Public School, Raniganj, India, GPA: 94%
2021 **AISSE**, DAV Public School, Raniganj, India, GPA: 96%

Technical Skills

Languages C, C++, Python, JavaScript
Data & Analytics SQL, DBMS, Data Structures & Algorithms, Statistical/Analytical Problem-Solving
Development HTML, CSS, JavaScript
Digital Design Verilog HDL, Digital & Analog Circuit Design, Computer Architecture
Tools Vivado, Multisim, CircuitMaker, LaTeX
Additional Cryptography & Secure Multi-Party Computation Fundamentals, Machine Learning Concepts
AI Tools Leveraged AI-assisted development tools to accelerate coding, debugging, documentation, and workflow automation, improving overall development efficiency.

Experience

Jun 2026–Jul 2026 **Research Intern**, CRIS Lab, Indian Institute of Science (IISc), Bangalore, India

- Analyzed security models and protocol design principles for secure multi-party computation (MPC) systems under Prof. Arpita Patra, applying rigorous analytical frameworks to complex, unstructured research problems.
- Reviewed and summarized cryptography research papers, translating theoretical protocols into structured, implementable concepts – applying advanced computational/algorithmic reasoning to real-world design constraints.
- Collaborated cross-functionally with PhD scholars and research associates in an active research group, aligning technical findings with broader project goals.
- Selected by faculty supervisor for invitation to Google Security Engineering Center (GSEC) India Research Day based on internship performance and analytical contribution.

Projects

Digital Logic Circuits Design, GitHub Repo

- Designed and implemented combinational and sequential digital logic circuits using Verilog HDL, applying systematic design and algorithmic thinking to build functional systems.
- Built control unit architectures modeling instruction sequencing, demonstrating ability to map problem requirements to technical solutions.
- Developed and executed test strategies via simulation and testbench validation in Xilinx Vivado.

Achievements

- Invited to Google Security Engineering Center (GSEC) India Research Day, Google Ananta, Bangalore (Jul 2026), engaging with Google researchers and academic leaders on AI safety, privacy, and cybersecurity.
- Scored 94% in AISSCE (PCM) and 96% in AISSE board examinations.
- Achieved 95 percentile in JEE Mains; secured Rank 962 in WBJEE.
- Led a 10-member team as Event Lead for Srijan (JUGS); awarded “Most Dedicated Volunteer.”
- Reached Top 24 nationally in India's Future Tycoons Season 3 (ENPOWER).